IN THE CLAIMS:

1. An integrated-circuit chip having one or more pairs of reversible wire-bonding-pads to alternatively provide a standard pattern for the reversible wire-bonding-pads and a non-standard, reversed wire-bonding pattern for the reversible wire-bonding-pads, comprising:

a first wire-bonding-pad;

a second wire-bonding-pad;

a first common signal line on said integrated-circuit chip;

a second common signal line on said integrated-circuit chip;

a first gate circuit having an input signal terminal connected to the first wire-bonding-pad, having an output signal terminal connected to the first common signal line, and having a control terminal which receives a standard wire-bonding configuration control signal which operates the first gate circuit to provide a standard pattern for the first wire-bonding-pad, which standard pattern connects the first wire-bonding-pad to the first common signal line to thereby provide the first input LOGIC signal to the first common signal line on said integrated-circuit chip;

a second gate circuit having an input signal terminal also connected to the first wire-bonding-pad, having an output signal terminal connected to the second common signal line, and having a control terminal which receives a non-standard, reversed wire-bonding configuration control signal which operates the second gate circuit to alternatively provide a non-standard, reversed pattern for the first wire-bonding-pad, which non-standard, reversed pattern connects the first wire-bonding-pad to the second common signal line to thereby alternatively provide the first input LOGIC signal to the second common signal line on said integrated-circuit chip;

a third gate circuit having an input signal terminal connected to the second wire-bonding-pad, having an output signal terminal connected to the second common signal line, and having a control terminal which receives the standard wire-bonding configuration control signal which operates the third gate circuit to provide a standard pattern for the second wire-bonding-pad, which standard pattern connects the second wire-bonding-pad to the second common signal line to thereby provide the second input LOGIC signal to the second common signal line on said integrated-circuit chip;

a fourth gate circuit having an input signal terminal also connected to the second wire-bonding-pad, having an output signal terminal connected to the first common signal line, and having a control terminal which receives the non-standard, reversed wire-bonding configuration control signal which operates the fourth gate circuit to alternatively provide a non-standard, reversed pattern for the second wire-bonding-pad, which non-standard, reversed pattern connects the second wire-bonding-pad to the first common signal line to thereby alternatively provide the second input LOGIC signal to the first common signal line on said integrated-circuit chip;

wherein the first gate circuit and the third gate circuit are controlled by the standard-bonding-pad control signal to provide a predetermined standard bonding-pad configuration for the integrated-circuit chip, which standard bonding-pad configuration connects the first wire-bonding input pad to the first common signal line on the integrated-circuit chip and which standard bonding-pad configuration also connects the second wire-bonding-pad to the second common signal line; and

whereby the second gate circuit and the fourth gate circuit are controlled by the reverse-bonding-pad control signal to provide a predetermined alternative reversed bonding-pad configuration for the integrated-circuit chip, which alternative reversed bonding-pad configuration connects the first wire-bonding-pad to the second common

signal line and which alternative reversed bonding-pad configuration also connects the second wire-bonding-pad to first common signal line.

2. The integrated-circuit chip of Claim 1, including

a plurality of pairs of first and second wire-bonding-pads;

a plurality of pairs of first and second common signal lines which are associated with one of said first and second wire bonding-pads;

a plurality of pairs of first and second gate circuits which are associated with one of said first and second wire bonding-pads;

a plurality of pairs of third and fourth gate circuits which are associated with one of said first and second wire bonding-pads; and

wherein each of said plurality of pairs of first and second wire-bonding-pads provides a standard pattern and a non-standard, reversed pattern for each of said plurality of pairs of wire-bonding-pads for the integrated-circuit chip.

3. The integrated-circuit chip of Claim 1, including

a bonding-option wire-bonding-pad adapted to having an external voltage applied thereto to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or alternatively, wither the integrated-circuit chip is to provide a reversed path for the reversible wire-bonding-pads;

a voltage sensor circuit for sensing the voltage applied to the bonding-option wire-bonding-pad and for alternatively generating either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.

4. The integrated-circuit chip of Claim 3, including

two or more bonding-option wire-bonding-pads, each of which are adapted to having an external voltage applied thereto;

one or more voltage sensor circuits for respectively sensing the voltage applied to a respective bonding-option wire-bonding-pad;

a bonding option logic signal array for generating one or more bonding option logic signals; and

a logic circuit for generating standard NRO and non-standard, reversed RO gate control signals from the one or more bonding option logic signals.

5. The integrated-circuit chip of Claim 4, including three bonding-option wire-bonding-pads which are adapted to having an external voltage applied thereto such that the logic circuit for generating standard NRO and non-standard, reversed RO gate control signals generates the standard NRO and non-standard, reversed RO gate control signals.

6. The integrated-circuit chip of Claim 1 wherein the gate circuits includes a logic circuit which has a first signal input terminal connected to one of the wire-bonding-pads, which has a second control signal input terminal which receives a wire-bonding configuration control signal to operate the gate circuit, and which has an output terminal coupled to one of the common signal lines.

7. The integrated-circuit chip of Claim 6 wherein the gate circuits include a chip enable input terminal for receiving a chip enable signal CE to activate the gate circuits

8. The integrated-circuit chip of Claim 6:

wherein the logic circuit includes a first logic gate, having an input terminal connected to a first signal input terminal, having a second input terminal connected to the second control signal input terminal, and having an output terminal connected to an input terminal of the output driver circuit; and

wherein the logic circuit includes a second logic gate, having an input terminal connected through an inverter to the first signal input terminal, having a second input terminal connected through an inverter to the second control signal input terminal, and having an output terminal connected to an input terminal of the output driver circuit.

9. The integrated-circuit chip of Claim 8 wherein the first logic gate includes a NAND gate and wherein the second logic gate includes a NOR gate.

10. The integrated-circuit chip of Claim 9 wherein the first logic gate has an input terminal for receiving a chip enable signal CE and wherein the second logic gate has an input terminal for receiving an inverted chip enable signal.

11. The integrated-circuit chip of Claim 9 wherein the logic circuit includes an output driver circuit having an input terminal and having an output terminal connected to one of the common signal lines.

12. The integrated-circuit chip of Claim 11 wherein the output driver circuit includes a complementary-transistor output amplifier.

13. The integrated-circuit chip of Claim 12 wherein the complementary transistor amplifier includes a p-channel transistor having a gate terminal connected to an output terminal of the NAND gate and a N-channel transistor connected to an output terminal of the NOR gate.

14. The integrated-circuit chip of Claim 1 wherein the first and the second wire-bonding-pads are adapted to be connected to external control signals for the integrated-circuit chip.

15. A dual-die, double-sized, back-to-back, wire-bonded integrated-circuit chip assembly, comprising:

a first chip having one or more reversible wire-bonding-pads; and

a second chip having one or more reversible wire-bonding-pads wherein the chips are adapted to be centrally mounted back-to-back within a lead frame having inwardly-extending bonding fingers with one of said chips having its wire-bonding-pads reversed such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame.

16. The integrated-circuit chip assembly of Claim 15, including:

a bonding-option wire-bonding-pad adapted to having an external voltage applied thereto to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or

alternatively, whether the integrated-circuit chip is to provide a reversed path for the reversible wire-bonding-pads; and

a voltage sensor circuit for sensing the voltage applied to the bonding-option wire-bonding-pad and for alternatively generating either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.

17. The integrated-circuit chip assembly of Claim 16, including:

two or more bonding-option wire-bonding-pads, each of which are adapted to having an external voltage applied thereto;

one or more voltage sensor circuits for respectively sensing the voltage applied to a respective bonding-option wire-bonding-pad;

a bonding option logic signal array for generating one or more bonding option logic signals; and

a logic circuit for generating standard NRO and non-standard, reversed RO gate control signals from the one or more bonding option logic signals.

18. The integrated-circuit chip assembly of Claim 15, wherein the gate circuits include a complementary-transistor output amplifier.

19. The integrated-circuit chip assembly of Claim 15, wherein the first and the second chip are fabricated with the same mask sets to be identical chips and wherein one of said pair of identical chip are reversed when assembled back-to-back to the other chip of the identified pair such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame.

20. A method of providing a dual-die, double-sized, back-to-back integrated-circuit chip assembly, comprising the steps of:

providing a pair of integrated-circuit chips where a first chip has one or more pairs of reversible wire-bonding-pads;

providing an identical second chip also having one or more pairs of reversible wire-bonding-pads;

mounting two of the same integrated-circuit chips back-to-back;

reversing the internal connections to the wire-bonding-pads on one of the reversible integrated-circuit chips so that pads for similar functions are located near each other for wire-bonding; and

whereby identical integrated-circuit chips are used to provide a double-sized, back-to-back integrated-circuit chip assembly.

21. The method of Claim 20 wherein the two integrated-circuit chips are fabricated with the same mask sets.

22. The method of Claim 20 wherein the step of reversing the internal connection to the wire-bonding-pads of one of the reversible integrated-circuit chips includes the steps of:

selectively connecting a first wire-bonding-pad to the internal circuits usually connected to internal circuits for a second wire-bonding-pad; and

selectively connecting a second wire-bonding-pad to the internal circuits usually connected to internal circuits for the first wire-bonding-pad.